

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Appellant:	Andrew H. Barr et al.	Examiner:	Aditya S. Bhat
Serial No.:	10/714,386	Group Art Unit:	2863
Filed:	Nov. 14, 2003	Docket No.:	200308581-1
Title:	SYSTEM AND METHOD FOR TESTING A MEMORY WITH AN EXPANSION CARD USING DMA		

REPLY BRIEF TO EXAMINER'S ANSWER

Mail Stop Appeal Brief – Patents

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This Reply Brief is presented in response to the Examiner's Answer mailed Aug. 6 (hereafter Examiner's Answer), 2008, and in support of the Notice of Appeal filed Feb. 21, 2008 and the Appeal Brief filed May 20, 2008 (hereafter Appeal Brief), appealing the rejection of claims 1-20 of the above-identified application as set forth in the Final Office Action mailed Jan. 11, 2008.

At any time during the pendency of this application, please charge any fees required or credit any overpayment due to Deposit Account No. 08-2025 pursuant to 37 C.F.R. 1.25. Additionally, please charge any fees required to Deposit Account No. 08-2025 under 37 C.F.R. 1.16, 1.17, 1.19, 1.20 and 1.21.

Appellant respectfully requests reconsideration and reversal of the Examiner's rejection of pending claims 1-20.

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ARGUMENT

I. The Applicable Law

The Applicable Law is provided in the Appeal Brief.

II. Rejection of Claims 1-20 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent Publication No. 2003/0115385 (Adamane).

Adamane does not teach or suggest all of the limitations of claims 1-20.

A. Rejection of Claims 1-8 under 35 U.S.C. §103(a) as being unpatentable over Adamane

As described in the Appeal Brief, Adamane does not teach or suggest “a test module card directly coupled to the first expansion slot”, “wherein the test module card is configured to obtain access to a portion of the memory from the operating system” or “wherein the test module card is configured to cause tests to be performed on the portion of the memory using direct memory access (DMA) subsequent to obtaining access to the portion of the memory” as recited in claim 1.

In the Examiner’s Answer, the Examiner repeatedly states that Adamane teaches or suggest “wherein the test module card is configured to obtain access to a portion of the memory from the operating system” as recited in claim 1 without demonstrating a clear teaching or suggestion in Adamane of such a feature. See Examiner’s Answer, pp. 10 & 13-14.

On page 10, the Examiner states the following.

Paragraph 15 of the Adamane et al. reference clearly teaches input/output (I/O) devices (test card is an I/O device) that are configured to obtain access to a portion of the memory from the operating system. Further it should be noted that the computer architecture in both the prior art and appellant’s invention require some sort of operating system in order to test the memory. An operating system is merely a set of instructions that enable the computer hardware to perform desired functions. Therefore, it would be inherent for both the system (sic) to have an operating system as they are both performing a function.

On pages 13-14, the Examiner states the following.

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Note paragraph 0011 of Adamane et al. [cited portion omitted] clearly illustrates that the processors use function descriptive material i.e. computer programs and information structures in order to impart functionality to a computer system. As previously discussed a (sic) operating system is merely a set of instructions that impart functionality. Paragraph 0015 of Adamane et al. (see above) teaches that the I/O testing devices perform tests on the memory using direct memory access (DMA). Clearly, a portion if not all the memory is accessed as it is being tested. Furthermore, the operating system/functional descriptive material must be stored in a memory and the memory is what is being tested. Please refer to Paragraph 0011 recites (sic) “processors 100 process functional descriptive material that is encoded into a computer readable medium such as main memory 106” (sic)

It is the examiners (sic) position that the Adamane et al. reference teaches the test module card is configured to obtain access to a portion of the memory from the operating system.

Even assuming *arguendo* that paragraphs [0011] and [0015] of Adamane expressly or inherently teach *the existence* an operating system in the system of Adamane, paragraphs [0011] and [0015] do not teach or suggest that I/O devices 118 are configured to obtain access to a portion of cache memory 104 or main memory 106 from the alleged operating system. As noted in the Appeal Brief, paragraph [0015] of Adamane does not describe any interaction between I/O devices 118 and an operating system. Paragraph [0011] of Adamane does not even mention I/O devices 118 much less any interaction between I/O devices 118 and an operating system.

The Examiner has gone to great lengths in the above statements to establish the existence of an operating system in Adamane. The question, however, with regard to the rejection under 35 U.S.C. §103(a) is whether Adamane teaches or suggests the recited feature of claim 1. Instead of identifying a teaching or suggestion of “wherein the test module card is configured to obtain access to a portion of the memory from the operating system” as recited in claim 1, the Examiner only provides unsupported assertions that the above feature of claim 1 are present in Adamane. These unsupported assertions are insufficient to demonstrate a teaching or suggestion of the above feature of claim 1.

The Examiner also distorts the teaching of Adamane in attempting to show a teaching or suggest of the above feature of claim 1. The Examiner states that “[p]aragraph 0015 of Adamane et al. (see above) teaches that the I/O testing devices perform tests on the memory

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using direct memory access (DMA)” Examiner’s Answer, p. 13. While paragraph [0015] of Adamane may support the notion that tests are performed *using* cache memory 104 and main memory 106 in Adamane, Adamane does not teach or suggest that the cache memory 104 or main memory 106 themselves are tested. For example, Adamane does not provide any teaching or suggestion of how a failure of cache memory 104 or main memory 106 would be detected as would be expected if cache memory 104 or main memory 106 was being tested. Instead, Adamane teaches that “[t]he present invention provides a method, computer program product, input/output device, and computer system for stress testing the I/O subsystem of a computer system.” Adamane, paragraph [0005], lines 1-3 (emphasis added).

The above statement represents a distortion of the teaching of Adamane and does not support the notion that Adamane teaches the above feature of claim 1. The above statement does not identify any interaction between cache memory 104, main memory 106, or I/O devices 118 and an operating system. Accordingly, the statement fails to provide any indication of a teaching or suggestion by Adamane of “wherein the test module card is configured to obtain access to a portion of the memory from the operating system” as recited in claim 1.

In addition, the Examiner has again failed to identify a teaching or suggestion in Adamane of “wherein the test module card is configured *to cause tests to be performed on the portion of the memory* using direct memory access (DMA) subsequent to obtaining access to the portion of the memory” as recited in claim 1 (emphasis added). While paragraph [0015] of Adamane may support the notion of testing an I/O subsystem using cache memory 104 as described in paragraph [0005] of Adamane, paragraph [0015] does not teach or suggest that the cache memory 104 or main memory 106 themselves are tested.

Adamane does not teach or suggest the above features of claim 1. Accordingly, Appellant respectfully requests the reversal of the rejection of claim 1 and claims 2-8 which depend from claim 1 under 35 U.S.C. §103(a) for at least these additional reasons.

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B. Rejection of Claims 9-14 under 35 U.S.C. §103(a) as being unpatentable over Adamane

As described in the Appeal Brief, Adamane does not teach or suggest “obtaining access to a portion of a memory of a computer system from an operating system during operation of a computer system” as recited in claim 9.

Appellents respectfully submit that Adamane does not teach or suggest this feature of claim 9 for the additional reasons given above for claim 1. In addition, the additional citations to Adamane given in the Examiner’s Answer (i.e., paragraphs [0021] and [0022]) do not describe any interaction between I/O devices 200 and an operating system. Accordingly, paragraphs [0021] and [0022] of Adamane do not teach or suggest the above feature of claim 9.

Adamane does not teach or suggest the above features of claim 9. Accordingly, Appellant respectfully requests the reversal of the rejection of claim 9 and claims 10-14 which depend from claim 9 under 35 U.S.C. §103(a) for at least these additional reasons.

C. Rejection of Claims 15-20 under 35 U.S.C. §103(a) as being unpatentable over Adamane

As described in the Appeal Brief, Adamane does not teach or suggest “a test module card directly coupled to the expansion slot”, “wherein the test module card is configured to obtain access to a portion of the memory from an operating system”, or “wherein the test module card is configured to cause tests to be performed on the portion of the memory by providing read transactions associated with the memory to the I/O controller subsequent to obtaining access to the portion of the memory” as recited in claim 15.

Appellents respectfully submit that Adamane does not teach or suggest these features of claim 15 for the additional reasons given above for claim 1. Accordingly, Appellents respectfully requests the reversal of the rejection of claim 15 and claims 16-20 which depend from claim 15 under 35 U.S.C. §103(a) for at least these additional reasons.

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CONCLUSION

For the above reasons, Appellants respectfully submit that claims 1-20 of the pending Application have not been established to be obvious in view of the cited reference.

Accordingly, Appellants respectfully request that the Examiner be reversed.

Any inquiry regarding this Reply Brief should be directed to either Christopher P. Kosh at Telephone No. (512) 241-2403, Facsimile No. (512) 241-2409 or David A. Plettner at Telephone No. (408) 447-3013, Facsimile No. (408) 447-0854. In addition, all correspondence should continue to be directed to the following address:

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Respectfully submitted,

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